

# Complementary high-speed SiGe and CMOS buffers

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## 1. Introduction

This chapter on high speed buffers in complementary SiGe and CMOS technologies studies three different buffer application areas, that is PA-driving, balun buffers, and finally LNAs. The underlying idea of this text is to point out the benefits obtainable from the application of complementary analog signal processing techniques. More specifically, the text will study applications of the inverter-like continuously biased current-reuse stage in different buffering purposes. One implementation example is shown in the attached Fig. 1, where a continuously current-biased gain cell uses the complementary PMOS to generate extra transconductance. A challenge for microwave applications of this current-reuse cell is to find ways to deal with the added parasitic capacitance associated with the complementary device.

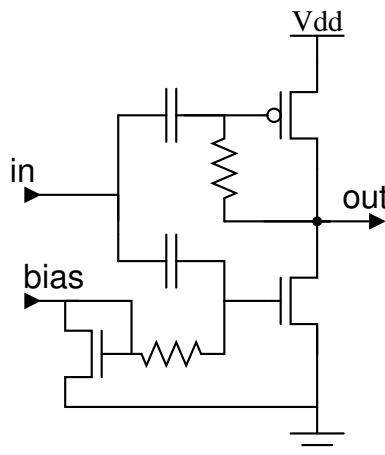


Fig. 1. A CMOS current-reuse cell.

First the reader will be introduced to the subject through a review on complementary bipolar devices in Section 2, including a discussion on a 10-GHz SiGe version of the “compound” emitter-follower. Integrated buffers with balun functionality will follow next in Section 3,

where the reader focus is directed towards FET technologies. Albeit most of the baluns presented in this section have originally been implemented in GaAs, they are realizable in CMOS technologies which have lately emerged as a viable microwave technology due to the radical scaling of the minimum realizable linewidths in this planar technology. The balun section serves as an introduction to Section 4 on different CMOS low-noise amplifiers (LNA), and this includes results on a 130-nm CMOS LNA as realized by the author. Summary of the findings will conclude this chapter.

## 2. Complementary bipolar devices and applications

Different complementary bipolar technologies have been known for decades, e.g., Davis used a complementary compound emitter-follower stage as an inter-stage push-pull OpAmp buffer in Davis et al. (1974). Despite this early success, interest in this niche of semiconductor business really picked up after Texas Instruments introduced a modern 0.4- $\mu\text{m}$  complementary SiGe process variant by El-Kareh et al. (2003). Author and his student Mr. Pellikka were able to experiment with this technology in 2006, when they realized a high dynamic range (DR) current reuse mixer and a linear push-pull buffer with an active area of 0.11mm $\times$ 0.1mm for base station applications in this 5-V complementary 0.4- $\mu\text{m}$  SiGe process. At 2 GHz, the realized mixer achieves a nominal measured dynamic range (DR) of +154 dB, while drawing 29 mA from a 3.3-V supply, whereas the push-pull buffer has an output-referred 1-dB compression point ( $OP_{1dB}$ ) of +9 dBm, while drawing 33 mA from a 5-V supply. This text will be limited to a discussion of this push-pull buffering circuit.

The initial reason for this study has been the fact that base station transmitters for 3G wireless standards require linear buffer stages to be installed after the IQ-modulator to boost the transmitted signal before the PA so as to produce high power transmissions without unacceptable spectral splatter. This leads to an increased bill of materials (BOM) and to increased power dissipation. To minimize the number of the expensive discrete buffers, it is advantageous to maximize linear output power of the IQ-modulator itself. High linearity is of increased importance due to the variable envelope modulations adopted for high bitrate performance in the emerging wireless standards. One such modulation format is OFDM, which entails an envelope variation with a peak-to-average ratio (PAR) of 8-13 dB. Transmitted noise should also be kept as low as possible, since it defines the smallest possible signal which can be transmitted. A complementary bipolar technology could help the designer to meet these requirements: a recently developed SiGe variant by El-Kareh et al. (2003) on a silicon-on-insulator (SOI) substrate has the necessary speed for most commercial applications below 3 GHz, as its  $f_T$ 's are at 18 and 19 GHz for the NPN- and PNP-transistors, respectively. The quoted  $f_T$ 's, in combination with a SOI-substrate make possible the definition of additional design goals: 1) broadband performance for use in multi-purpose radios; 2) use of integrated coils should be avoided so as to minimize RFIC-area, and, 3) operation at low supply voltages should be possible. The last point is somewhat contradictory, since on the other hand it is good to dissipate less power as this makes design of the system power budget more relaxed, but on the other hand it should be noted that a high output power and robust circuit operation is fundamentally important in basestations. In this regard, the chosen 5-V complementary SiGe process has an advantage over the predominant complementary technology, the submicron CMOS, which currently typically withstands 1.2-V supplies. Also no reports on negative bias temperature instability (NBTI) has been filed on the SiGe technology, and lack of this CMOS hazard as reported by, e.g., Peters (2004) should improve the reliability of the designs in general. In response to these demands, this paper complements the abridged description

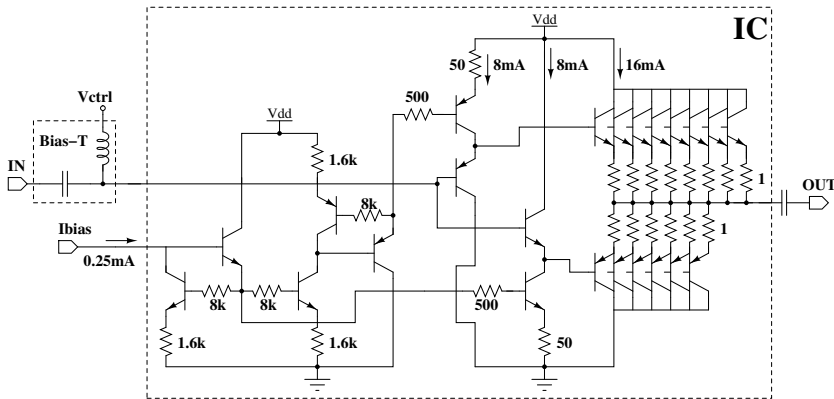


Fig. 2. Microwave push-pull buffer with ballasting resistors shown Tiiliharju & Pellikka (2007) (© 2007 IEEE).

given in Tiiliharju et al. (2006) of a broadband push-pull buffer realized in the complementary  $0.4\text{-}\mu\text{m}$  SiGe process.

### 2.1 Push-pull Buffer

The  $0.4\text{-}\mu\text{m}$  complementary SiGe technology can be used to extend the bandwidth of an emitter-follower push-pull stage from VHF to microwave frequencies with a high current drive capability similar to its predecessor which was reported as a *compound emitter-follower* in Davis et al. (1974) for inter-stage buffer use in a VHF operational amplifier. However, because of the insulating SOI substrate, there is a risk of thermal run-off in stages with high currents as noted by Monticelli (2004). This risk is a combination of two factors: 1) SOI-substrate reduces heat radiation away from the transistor, and 2) bipolar transistors have a *positive* thermal coefficient. Therefore, without feedback a warming bipolar transistor will draw more current, which makes the device warmer until this cycle leads to its destruction. To prevent this, local feedback has been introduced as each output stage emitter stripe has been ballasted with a single  $1\text{-}\Omega$  metal path resistor. This is shown in the schematic of Fig. 2 including biasing details and emitter-follower drivers for this complementary output stage. A bias-T and a dc-blocking capacitor have been used for circuit measurements, and these have been depicted in the Fig. outside the IC dashed box. A pair of these buffering circuits have been realized on the final IC to accommodate for possibly needed differential measurements with external connectorized baluns, and this is shown in the micrograph of Fig. 3. However, the results reported herewith have been extracted using a single device, unless otherwise noted.

Design simulations for this circuit indicate thermal stability, and with the  $250\text{-}\mu\text{A}$  biasing current, the nominal performance includes a three decibel bandwidth ( $BW_{3dB}$ ) of 11 GHz, and an  $OP_{1dB}$  of +11 dBm, while the circuit dissipates 33 mA from the 5-V supply used. Next section will give measurement results and compares those with the simulated performance to validate the design methods used.

### 2.2 Push-pull IC realization

Micrograph of the realized complementary SiGe push-pull buffer pair is shown in Fig. 3, and the standard  $150\text{-}\mu\text{m}$  pitch gsgsg probe pad layout depicted underlines the compact size

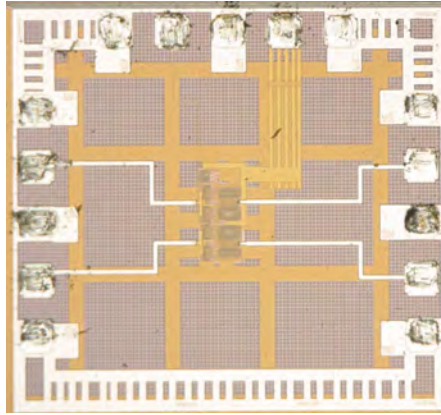


Fig. 3. Micrograph of the realized 10-GHz highly linear push-pull buffer pair.

achieved with this inductorless broadband circuit technique. In this microwave frequency measurement technique, g stands for a ground, s for a signal pad, and the deep probing marks on the pads have been inflicted during a thorough testing of the chip.

The measured insertion gain  $S_{21}$  of the push-pull stage at the chosen nominal biasing point of 33 mA from a 5-V supply is shown in Fig. 4 with a realized  $BW_{3dB}=9.5$  GHz. Other measured data extracted using a 2 GHz signal frequency includes:  $OP_{1dB}=+9$  dBm, and  $NF=5$  dB, whereas the second and third harmonic products lie at -48 dBc and -54 dBc in relation to the chosen nominal 0 dBm output power. Two tones with a 10-MHz separation have been used to extract an output-referred third-order intercept point  $OIP3=+22$  dBm. Combined these values reveal that good linearity and noise performance have been achieved without coils, since typically this level of performance requires the use of a distributed amplifier with a multitude of integrated coils, which increases the IC-area to 4-80 times that of the push-pull stage. In fact, the  $0.11\text{mm}\times 0.24\text{mm}$  active area prototype contains two push-pull stages and their shared biasing. A single push-pull measures  $0.11\text{mm}\times 0.1\text{mm}$ . In-all, small IC area and high linearity ( $OIP3=+22$  dBm) of the push-pull stage suggest use in broadband high output power IC's.

The measured push-pull data matches simulated values reasonably well at the same operating point with exact matches on  $S_{21}=6$  dB,  $P_{OUT}=0$  dBm, and  $2ND\text{-rej}=-48$  dBc; the remaining differences can be listed with simulated values in parentheses as:  $BW=9.5(11)$  GHz,  $2ND\text{-rej}=-54(-57)$  dBc,  $OP_{1dB}=+9(+11)$  dBm, and  $NF=5(4)$  dB. Therefore the simulated values can be used to compare the proposed current-reuse push-pull buffer to the more commonly used emitter-follower buffer realized with NPN-transistors. This emitter-follower, or common-collector (CC), reference stage has also been realized as a cascade of two CC-stages at a similar biasing point and  $P_{OUT}$ . The data is shown in Table 1 with separate columns for the simulated values. Comparison of the simulated results predicts a +12-dB improvement in harmonics attenuation for the push-pull stage at the 2-GHz test frequency. This improvement in linearity is confirmed by the predicted increase in  $OP_{1dB}$  of +4 dB for the push-pull stage, and it is due to the increased current drive capability of the implemented complementary circuitry. Penalty for this linearity increase is a simulated 4-GHz drop in BW as the push-pull BW of 11 GHz is compared to the CC-reference BW of 15 GHz.

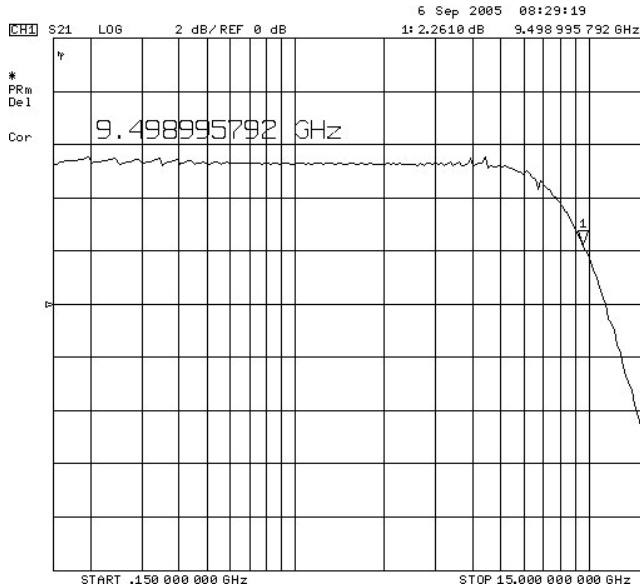


Fig. 4. Measured push pull stage insertion gain  $S_{21}$  at 33 mA/5  $V_{DD}$  nominal operating point Tiiliharju & Pellikka (2007) (© 2007 IEEE).

To test for possible thermal run-off, a pair of close-lying push-pull stages was biased at almost twice the nominal current of 33 mA to dissipate 300 mW each from the 5-V supply: as a result a gain stability of  $\pm 0.1$  dB was measured during a period of 18 h with no traces of thermal run-off. Since a corresponding 12-h current dissipation measurement gave  $I_{DD}$  variation at  $59.8 \pm 0.3$  mA, it is safe to conclude that thermal run-off can be prevented by ballasting despite the insulating SOI substrate used.

So to conclude this section, it can be said that a successful extension of the push-pull buffer to gigahertz frequencies has been accomplished while high linearity and output drive have been maintained. However, transforming this design to other technologies such as CMOS is not a straightforward task and it is not clear whether this circuit technique could be utilized in modern nanometer CMOS designs. That said, the following section will shift focus towards CMOS technologies with a discussion on buffers with balun functionality.

### 3. Buffers with balun functionality

Most, if not all, communication transceivers utilize differential signaling, whereas antenna connectivity is single-ended. This means that a balun circuit needs to be employed to transform between these two signaling forms, and for economical reasons such a device should be implemented on-chip as connectorized balun hybrids operating at micro/millimeter wave frequencies are expensive devices. Also integrated balun performance might be better, as good intra-die element matching is one of the major driving forces behind the success of the integrated circuit technologies. This is illustrated by measured amplitude ( $\Delta A$ ) and phase ( $\Delta \phi$ ) errors shown in Fig. 5, where differential signaling deviations from ideal have been recorded. Three high-performance hybrids for the frequency bands of #1: 0.05-1 GHz, #2: 1-2 GHz, and

Table 1. Comparison of push-pull to a cascaded CC-stage.

		CC-CC*	Push-pull*	Push-pull
A	dB	5	6	6
$BW_{3dB}$	GHz	15	11	9.5
$P_{OUT}$	dBm	0	0	0
2ND-rej	dBc	-36	-48	-48
3RD-rej	dBc	-42	-57	-54
$OP_{1dB}$	dBm	+7	+11	+9
$OIP_3$	dBm	-	-	+22
NF	dB	4	4	5
$I_{DD}$	mA	32	33	33
$V_{DD}$	V	5	5	5

\* simulated results

#3: 2-4 GHz have been measured for this plot. In this Fig., the phase deviation from the ideal  $180^\circ$  is already fairly pronounced in the band of 1-2 GHz. Therefore, this section first catalogues known differential pair based balun implementations, then moves towards CMOS baluns via a discussion on different FET-based baluns. The latter mainly discusses known work in GaAs-technologies, but these are fully realizable in current CMOS technologies. This material already includes the basic topology used in one of the recently most-reported ultra-wideband (UWB) LNA topologies, that is, the noise-canceling LNA. That said, it should be noted that prior theoretical as well as intuitive proof on the superior balun performance of the differential pair baluns has been given by Altes et al. (1986); Tiiliharju & Halonen (2005), but that its noise and distortion performance is often unsatisfactory and forces use of the other balun techniques detailed herewith.

	$\Delta A$ [dB]	$\Delta\phi$ [deg.]	BW [GHz]	$S_{21}$ [dB]	$I_{DD}$ [mA]	$V_{DD}$ [V]	Process [ $\mu\text{m}$ ]	Year
Tripodi & Brekelmans (2007)	0.9	3.5	< 1	23	33	1.2	0.09 (CMOS)	2007
Tiiliharju & Halonen (2005)	-1	1	0.4-3.7	7	23	2.5	0.8 (SiGe)	2003
Kawashima et al. (2003)	0.5	2	0.5-4	-5	NA	NA	0.3 (GaAs)	2003
Ma et al. (1998)	1	1	0.5-4	NA	3.8	3	0.5 (GaAs)	1998
Kobayashi (1996)	1	6	0.5-5	NA	NA	5	2 (GaAs)	1996
Altes et al. (1986)	0.25	1	0.2-5	NA	NA	NA	1.0 (GaAs)	1986

Table 2. Comparison of measured balun performances.

### 3.1 Differential pair baluns

Since any differential pair offers the possibility of implementing gain in the signal path, it should be the chosen starting-point for a lower microwave range phase-splitter implementation. Also its inherent balun operation, which is sometimes referred to as its common-mode rejection ratio (CMRR), makes it a natural reference for the balun performance that is realiz-

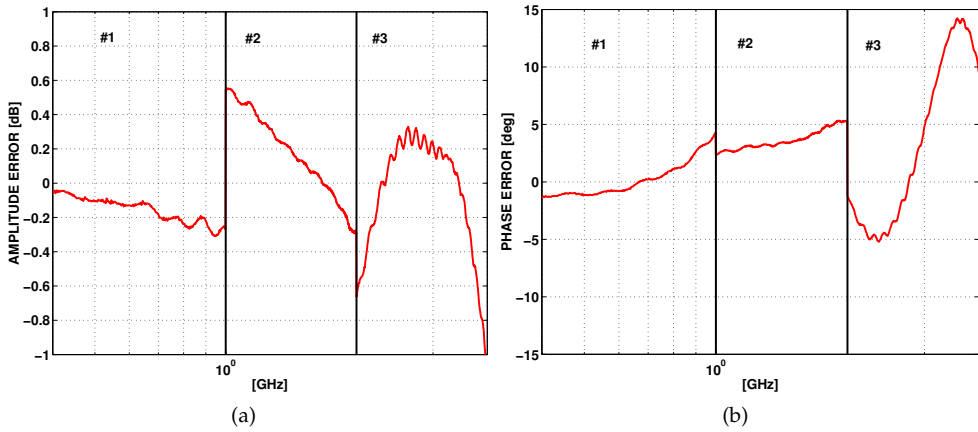


Fig. 5. Measured performance of three connectorized off-chip baluns in 0.4-4GHz.

able. A good bipolar implementation is the emitter-follower-driven differential pair shown in Fig. 6, with a reported performance of:  $\Delta A=1$  dB and  $\phi=180.7^\circ-186^\circ$  in 0.5-5 GHz.

A GaAs MESFET implementation is proposed by Ma et al. (1998), where an asymmetrical feedback LCR network is used as a means for improving differential pair phase-splitting performance to within  $\Delta A=\pm 1$  dB and  $\phi=180^\circ\pm 1^\circ$ . However, the proposed asymmetrical LCR feedback implementation shown in Fig. 7 makes achieving good broadband performance an intensive design task, as the LC feedback operates at a single resonance frequency, and location of this resonance is dependent on circuit parasitics, which depend on the supply voltages and the biasing point of the circuit.

To improve common-mode or even-order signal rejection, differential pairs can be cascaded: Altes et al. (1986) uses a single-transistor balun to drive a cascade of two differential pairs, as shown in Fig. 8. The circuit implementation achieves good phase-splitter performance at  $\Delta A=\pm 0.25$  dB and  $\phi=180^\circ\pm 1^\circ$  in 0.2-5 GHz. For this performance, a 1  $\mu\text{m}$  epitaxial GaAs MESFET technology with air bridges and MIM capacitors was used. This is a very interesting implementation as each cascaded balun theoretically improves differential signaling quality as shown by Tiiliharju & Halonen (2005), and as it deals with the known bad noise figure (NF) performance of the differential pair by driving a pair of them with a single transistor gain stage. The trick here is best revealed with the classic Friis' noise figure equation for cascaded systems, as it ties a cascade system noise figure to individual block noise figures as in:

$$NF = NF_1 + \frac{NF_2 - 1}{A_{P1}} + \frac{NF_3 - 1}{A_{P1}A_{P2}}, \quad (1)$$

where all factors are real, not in decibels, and the result is given in decibels. Numbering refers to stages from-left-right in Fig. 8, and factors  $A_{P(1,2,3)}$  stand for the available power gains of three amplifying stages shown.

The Friis' equation explicitly shows that by optimizing the first stage NF and gain  $A_{P(1)}$ , it can be made to dominate system noise characteristics whereas high cascaded gain nulls contribution from the following stages. However, at higher frequencies each active stage usually adds notably to power dissipation, and without feedback a high number of gain stages in a cascade

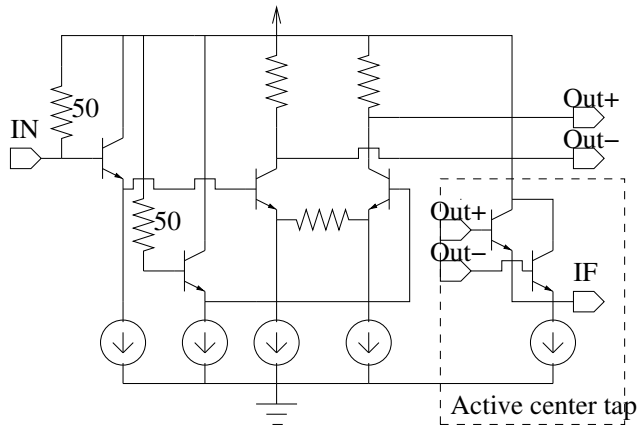


Fig. 6. Linearized emitter-follower driven differential pair reported as an integrated balun by Kobayashi (1996).

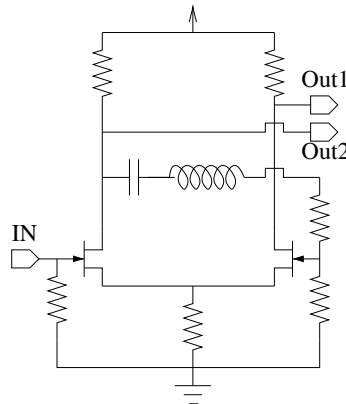


Fig. 7. A differential pair balun with a correcting feedback LCR-network by Ma et al. (1998).

will decrease circuit linearity. Furthermore, it has been shown by Fong & Meyer (1998) that a differential pair always has inferior linearity when compared to a similarly biased common-source stage, so this linearity-power tradeoff limits application of cascading in balun accuracy improvement.

### 3.2 Modified CGCS topology

A CGCS topology is defined as having a good broadband amplitude balance by Kawashima et al. (2003), while its phase difference is usually poor. In contrast, the modified CGCS topology shown in Fig. 9 realizes both good amplitude and phase balances with measured performance at:  $\Delta A=0.5$  dB and  $\phi=178^\circ-180.2^\circ$ . A problem with this implementation is the reported -5 dB loss performance per branch, despite the  $0.3\text{-}\mu\text{m}$  GaAs MESFET technology used. Nevertheless, this balun form has been known for decades, and it has also been used as a class-AB mixer input stage by Gilbert (1997), and in noise-canceling LNAs originally proposed by



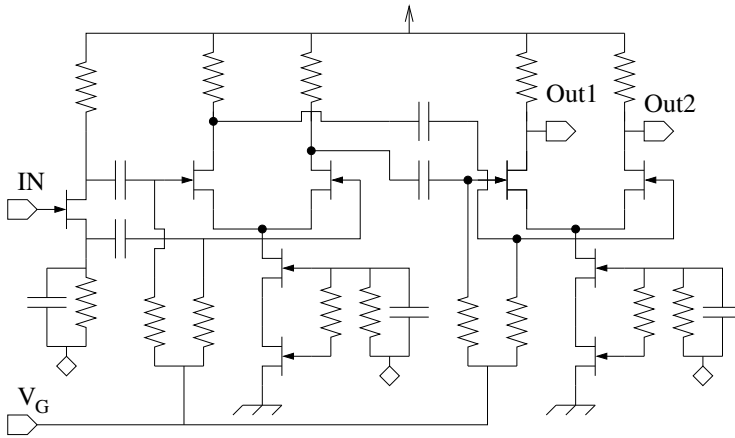


Fig. 8. Cascaded differential pairs used as a balun by Altes et al. (1986).

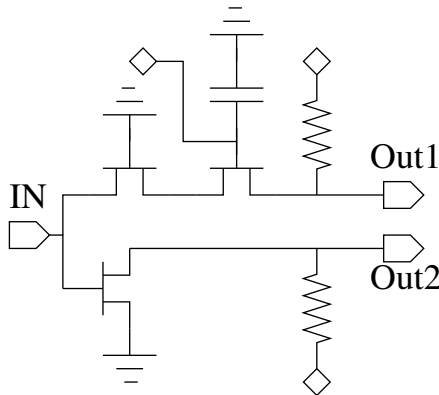


Fig. 9. The CGCS-balun principle developed by Kawashima et al. (2003).

Bruccoleri et al. (2002), a technique which has recently been favored by the UWB design community.

### 3.3 Single-transistor phase-splitters

Usually, single-transistor phase-splitters have too much phase error as a result of circuit parasitics. Fig. 10 depicts an example of a single transistor balun, where FET drain and source nodes are used as outputs; as is well-known, the inverting (drain) and non-inverting (source) node impedances differ substantially. The impedance seen at the drain node is formed by the parallel connection of the channel conductance  $g_o$  and several parasitic capacitances, such as the gate-to-drain  $C_{gd}$ , and drain-to-bulk  $C_{db}$  capacitances. In contrast, the device transconductance  $g_m$  seen at the source node is in most cases so high that it dominates circuit source impedance estimates. This inherent imbalance has a deleterious effect on the performance of a single FET circuit as a balun, and the reported  $\Delta A=1$  dB (gain error) and  $\phi=176^\circ$  (phase difference) values by Koizumi et al. (1995) are in agreement with this, as these *simulated* re-

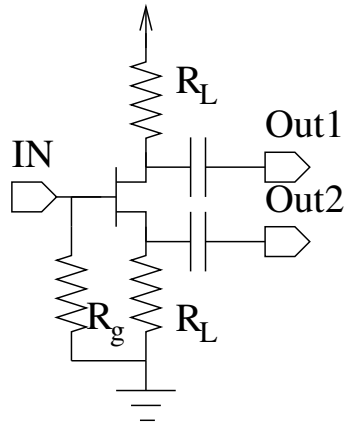


Fig. 10. One FET as a balun by Koizumi et al. (1995).

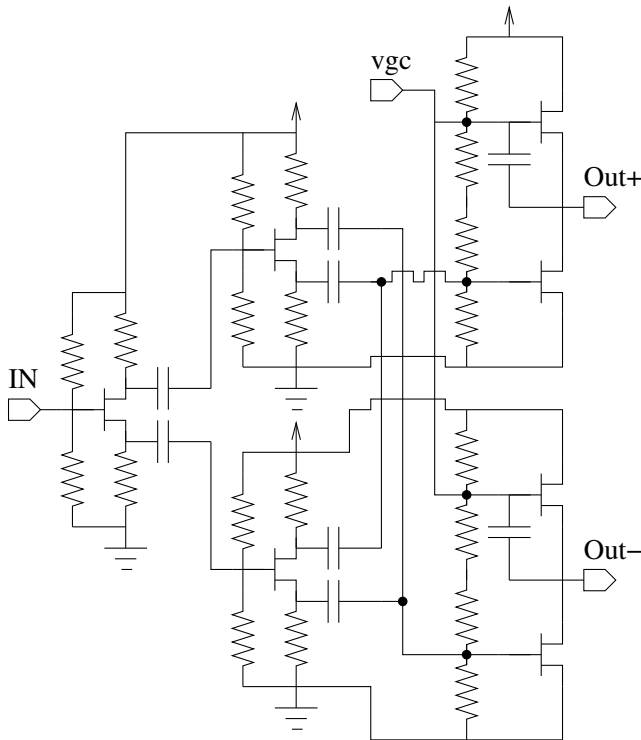


Fig. 11. Cross-connected FETs correct single FET balun response by Goldfarb et al. (1994).

sults were reported as best possible for a single FET balun optimized for use in a Personal Communication Systems (PCS) application at 950 MHz.

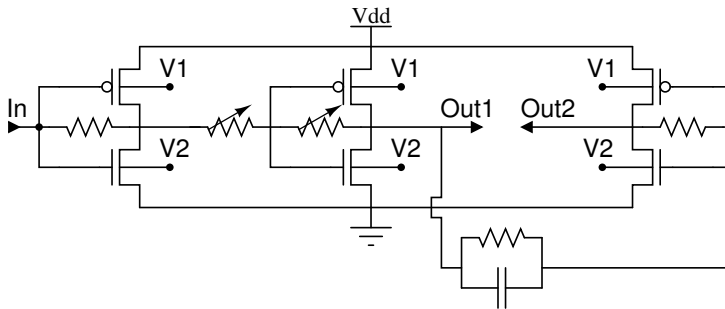


Fig. 12. One of the few balun amplifiers which exploits complementary circuit techniques made by Tripodi & Brekelmans (2007).

To correct the inherent imbalance of the single FET balun, Goldfarb et al. (1994) proposed the use of a pair of cross-connected correcting transistors, as shown in Fig. 11. However, this is not a promising candidate for a broadband balun solution, for two reasons: 1) seven integrated capacitors (excluding output buffering) are needed to make it work, so there is an increase in IC area and a great deal of parasitic capacitance involved, and 2) for better balance each transistor should have equal gain from the gate to the source/drain terminals: this limits the topology to use in low-gain applications. The combination of these two points does not imply good broadband performance for this topology, but the reported *simulated* gain and phase values from 1 GHz to 2 GHz support claims for improved accuracy:  $\Delta A = -0.2$  dB and  $\phi = 178^\circ$ .

### 3.4 Inverter balun amplifier

CMOS inverters have been successfully used to implement a balun variable gain amplifier (VGA) LNA for handheld mobile-TV applications by Tripodi & Brekelmans (2007). Schematic of this 90-nm CMOS LNA is shown in Fig. 12, and its use of inverters as gain stages has similarities with the feedback amplifier proposed by the author later in this chapter. However, important differences exist such as: a) biasing current control in Fig. 12 has been realized using the back-gate biasing voltages V1 and V2, b) use of a series-connected resistor has been avoided by the author to keep NF low, and c) the amplifier shown does not use a global feedback but uses local inverter stage feedback resistors instead. Tabulated results for this and the other baluns of this section in Table 2 miss many of the fine characteristics such as the rather low NF=2.5 dB realized for this low-noise VGA, but reference to the table is still an appropriate conclusion for this section and a fitting preliminary to the next section on LNAs. Based on the table, it is good to point out that well-used complementary stages not only give the best dynamic range performance but they also produce comparable functionality for most applications.

## 4. CMOS Low-noise amplifiers

It was long widely believed that short-channel CMOS application in high-speed low-noise amplifiers (LNA) would not be successful, as these devices have a higher than usual excess noise factor  $\gamma$ . However, that belief has been shown premeditated, first with sub-1dB noise figure LNA implementations for narrowband applications, then with emerging ultra-wideband (UWB) LNAs. Since ultra-wideband (UWB) technologies are currently gaining acceptance

also in European standardization bodies, this niche of communications is under active development worldwide.

Nevertheless, before plunging forward it is appropriate to limit our broadband LNA discussion to inductorless fully integrated designs according to the general layout of this chapter. It is also necessary to mention two specific items of interest: 1) the term LNA will be limited to low-noise amplifiers which have a gain higher than 10 dB, preferably more, and 2) noise figures are only acceptable in the band where the circuit's input has been matched to  $50\ \Omega$ . The first item stems from the very function of any LNA as defined by the Friis's formula: a low-noise amplifier has to have sufficient gain to isolate and to improve system noise figure, i.e., to make its own low NF the dominating factor in the system NF. The second item stems from the fact that it is trivial to achieve near GaAs-like NF-performances with large WL-area CMOS transistors which have not been matched to  $50\ \Omega$ , but this is a bit unrealistic, as applications usually dictate mandatory matching to  $50\ \Omega$ .

This section will first discuss existing feedback LNA solutions, then performance enhancing design techniques such as noise-canceling and current-reuse inputs will be presented, and this section will be concluded with implementation detail on an LNA by the author which uses current-reuse gain-stages in combination with a semi-active dual feedback loop to achieve low noise, high gain and good isolation in a 130-nm bulk digital CMOS technology.

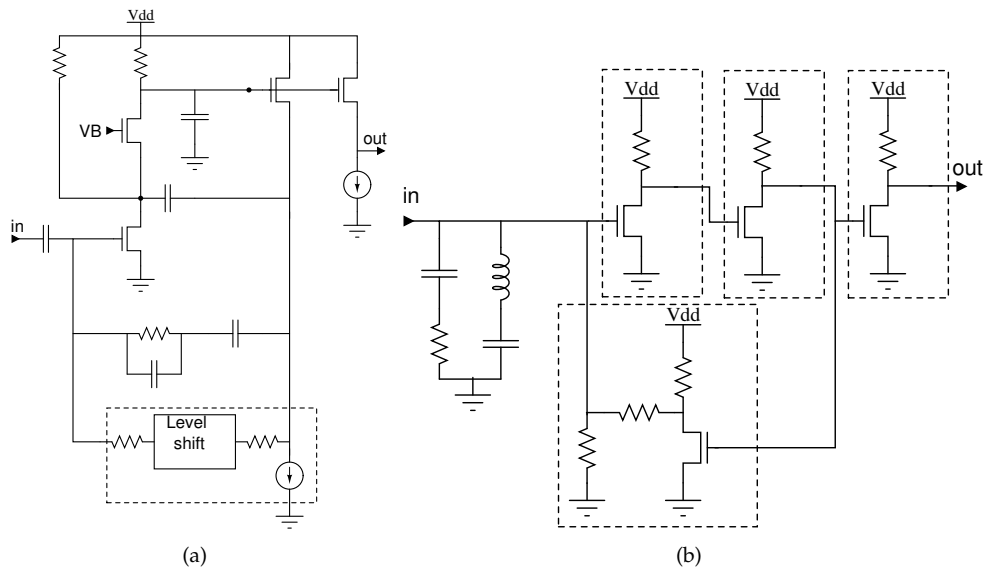


Fig. 13. Two noteworthy feedback LNAs.

#### 4.1 Feedback LNAs

For economical reasons a bulk CMOS process mainly intended for integration of digital circuitry should be used for the purpose of implementing LNAs. Sufficient bandwidth with little gain variation could be guaranteed with three alternative techniques: 1) distributed amplification, 2) use of a complex filtering network at circuit input/output, or 3) feedback amplification. First choice is generally limited by its higher power dissipation and possibly intensive

design effort, whereas the second choice includes an increased IC area, high design effort and resistive losses from parasitics. These considerations therefore suggest use of the third alternative, where a feedback network is used to swap amplifier gain for a wideband frequency response. Advantageously, this stabilizes gain and port impedances as well, and this well-known technology is compatible with low-cost integration in digital CMOS.

However, the amount of applicable feedback is limited by stability considerations, and this has traditionally been dealt with by using different compensation networks which aim at increasing the amount of available stable feedback. Conventional microwave feedback designs use complex compensating capacitor networks for the purpose, but this approach is area-consuming, sensitive to parasitics, and time-consuming to design. An example of a very complex feedback network is seen in Fig. 13(a) which is the single-stage UWB low-noise amplifier (LNA) design reported by Zhan & Taylor (2006). This high-performance low-noise amplifier (LNA) in 90-nm CMOS achieved inspiring performance with a best possible  $NF=2.5$  dB performance over the UWB bands. However, this particular implementation uses a 2.5-V supply voltage, and is therefore really not applicable for designs in standard digital CMOS as these use 1.2-V for 130-nm and as low as 1.0-V supplies for newer process nodes, as its use of stacked transistors limits the available dynamic range (DR), and its complex feedback network requires an involved design effort. Fundamentally limiting is the low intrinsic gain of digital transistors, which decreases a single stage gain to an unacceptably low level.

A possible alternative which uses three cascaded gain stages is shown in Fig. 13(b) as reported by Janssens et al. (1997), where the main idea is to improve isolation of the circuit by driving a resistive feedback network with a gain stage. The circuit in Fig. 13(b) is in fact a variation of a well-known bipolar amplifier connection where an emitter-follower is used to drive the feedback resistors connected to the input port. However, although the depicted connection is simple on the surface, its use for e.g. UWB applications is problematic as the feedback amplifier gain roll-off introduces difficult high frequency poles to the single feedback circuit. As a testimony to this the original circuit shown in Fig. 13(b) uses two additional impedance networks at its input to compensate for parasitic effects: an inductor and its dc-block have been applied to null parasitics, and a resistor-capacitor (RC) network has also been applied to ensure stability.

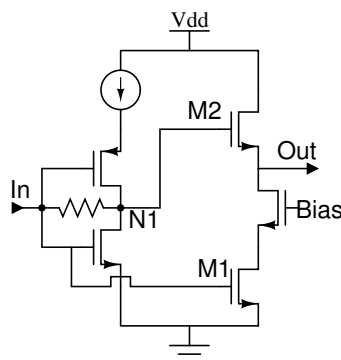


Fig. 14. A noise-canceling stage implementation with biasing details omitted for clarity.

## 4.2 Noise-canceling LNAs

A very popular broadband low-noise amplifier technique was proposed by Bruccoleri et al. (2002) to break the connection between input resistive matching and noise figure by exploiting two feedforward paths for the input-referred noise with matching transfer characteristics but opposite signs. A better understanding of the technique is possible with reference to Fig. 14, where the inverting noise feedforward path is via NMOS transistor M1, whereas the non-inverting noise path is via NMOS transistor M2. According to inventors, the trick here is that noise in nodes **In** and **N1** is in-phase as the same noise current flows through the feedback resistor R to the source impedance Rs (not shown). This is in contrast to signal phase, which gets inverted by the input stage, and therefore adds at circuit output.

Originally reported performance supports the proposed noise-canceling theory, as sub-2dB NF values with matched input have been reported in the band of 250-1100 MHz with good all-around performance. This performance is limited by the accuracy by which the two opposite phasing noise feedforward paths match both in magnitude and phase domain. Indeed, later implementations for higher frequencies tend to show worse NF value performance, e.g., best noise-canceling ultra-wideband LNAs reported in 2006-2007 (tabulated in the last subsection in Table 3) reach NF values of 2.7-5.5 dB. To understand this drop from expected low NF performance in many cases, it should be noted that matching of the two noise feedforward paths comes increasingly difficult at higher frequencies. Also use of nanometer CMOS devices, which have high channel conductances, makes it difficult to hold on to the assumption that M2 acts as a perfect 1/1 voltage-follower. Significance of this is better understood if the original matching condition is re-printed with the channel conductances taken into account:

$$A_{M1} = A_{M2} \iff \frac{g_{m1}}{g_{m2} + g_{d2}} = \left(1 + \frac{R}{R_s}\right) \frac{g_{m2}}{g_{m2} + g_{d2}}, \quad (2)$$

where  $A_{M(1,2)}$  are FET M1 and M2 associated signal path gains,  $g_{m(1,2)}$  are FET transconductances,  $g_{d2}$  represents all impedances at the output node, and the feedback and source impedance have been labeled as R and Rs, respectively.

A simple practical interpretation for this matching condition is as follows: since gain is needed to make the LNA noise performance the dominant one, both paths need to have a medium-to-high gain, a condition which dictates matching of a source-follower M2 transfer function with that of a common-source stage M1, including its Miller capacitance. This is clearly a very demanding task for broadband amplifiers.

Therefore, rest of the chapter will discuss possibilities to overcome feedback stability problems so as to fully utilize cascaded current-reuse amplifiers' gain in an ultra-wideband LNA application. This approach is somewhat prone to dissipate higher currents, but its application band should increase in direct relation to decreasing parasitics, i.e., this approach should scale well for nanometer CMOS use.

## 4.3 Current-reuse LNA with semi-active feedback

This section proposes a current-reuse LNA implementation with a semi-active dual feedback loop as reported by the author in (Tiiliharju & Koivisto (2008)) for the lower UWB band. The proposed LNA topology scalability to nanometer CMOS processes is good, and as a proof-of-concept it has been integrated in a 130-nm digital CMOS process. The proposed LNA can be mass-produced at a negligible cost with extremely small die area, as it utilizes an area-saving inductorless topology. Furthermore, its novel feedback stage improves isolation, increases stability, and slightly improves circuit noise performance with no discernible extra cost.

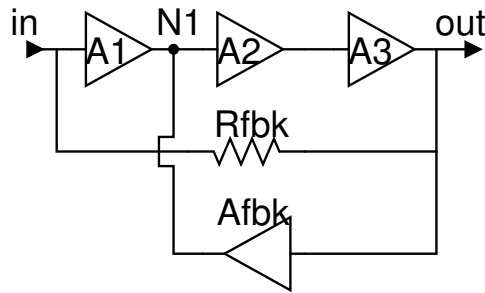


Fig. 15. Proposed feedback network application in a cascade amplifier.

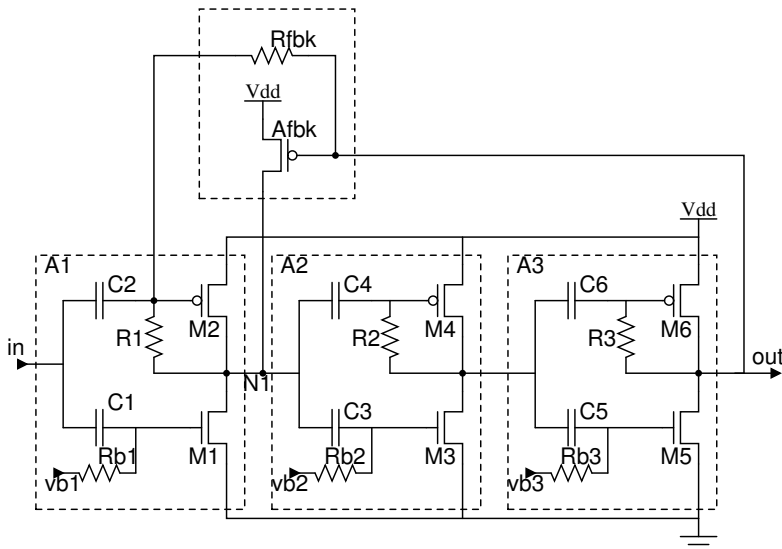


Fig. 16. Transistor level realization of the proposed feedback network application in an UWB LNA.

#### 4.3.1 Design and Architecture

Generally the amount of applicable feedback is limited by stability considerations, but the amount of available stable feedback can be increased by using an active stage Afbk to feed output signaling back to a first internal node N1 at the output of the first amplifier stage A1 of the cascade A1-A3, and also to its input port via a resistor connection as shown in Fig. 15. A copy of the last amplifier stage, or part thereof, could be used as the proposed active feedback stage as this allows accurate setting of the amount of feedback used by simple scaling of said dc-connected feedback stage. The proposed use of a copy of the last amplifier stage is the key behind increased amount of stable feedback available, as this inherently realizes frequency compensation by duplicating single amplifier pole and zero locations. Thus the well-known stability condition reported by Sedra & Smith (2003), which denies exceeding a 20-dB difference between the slopes of the amplifier and feedback frequency response curves

at the point of their Bode-plot intersection is naturally easier to meet. This preferred embodiment also avoids prior art (Janssens et al. (1997)) problem of loading the amplifier input port with feedback amplifier poles and zeros, and the designer can opt for the added flexibility of two feedback paths by realizing part of the desired feedback with a feedback resistor  $R_{fbk}$ , which is connected between the cascade amplifier input and output ports. Isolation is also increased and noise slightly decreased, since feedback resistor  $R_{fbk}$  values can be made larger or practically infinite for the same amount of feedback. This is a direct consequence of the smaller amount of feedback which has to be realized resistively for a given desired amount of feedback.

Fig. 16 shows proposed transistor-level realization of the wideband cascade amplifier implementation wherein feedback network ( $A_{fbk}$ ,  $R_{fbk}$ ) has been arranged to trade signal gain arising from the three amplifying stages A1-A3 to a wideband frequency response. Technology used for this implementation is a bulk 130-nm digital CMOS process with optional MIM capacitors used for dc-blocking, and a nominal supply of 1.2 volts. High-speed transistors with low threshold voltages at  $V_{TN0}=380$  mV for NMOS, and  $V_{TP0}=-390$  mV for PMOS variants have been used to build the three near identical core amplifier blocks A1, A2, and A3. All capacitors are 1.25-pF integrated MIMs except input capacitor C2 which has been realized as an off-chip capacitor. Local feedback and biasing resistors R1 and R3 at the input and output buffering amplifiers A1 and A3 have been set at a low value of  $400 \Omega$  to improve input match and to linearize the device at its output, whereas the second stage local feedback resistor R2 has been set to  $1200 \Omega$  to increase gain. Transistor M1-M6 areas have been set quite high to keep the noise figure floor of each stage at a low value; thus  $16 \times 8\mu m / 0.13\mu m$  has been given to each device, notwithstanding whether the device in question is a N- or a PMOS transistor. Traditionally PMOS-transistors with similar channel lengths L were allocated as much as three times the channel width W of their NMOS counterparts, but to cut down circuit parasitics this approach has now been avoided.

Based on previous knowledge and simulations each  $8\text{-}\mu m$  wide unit transistor has been realized in 4 fingers, as this configuration should help to minimize noise by keeping channel resistances at bay. The biasing resistors Rb1, Rb2, and Rb3 have no effect on broadband noise figure, as they have been given a high value at  $9.2 \text{ k}\Omega$  to exclude biasing chain from signal path and maximize gain. The feedback network devices have been set at  $A_{fbk}=8\mu m / 0.13\mu m / \text{PMOS}$ , and  $R_{fbk}=1.2 \text{ k}\Omega$ .

### 4.3.2 Simulated performance

The advantages of the proposed feedback network show more clearly with increasing amounts of feedback. To demonstrate this Fig. 17 depicts simulation results for two feedback amplifiers which trade gain from identical similarly biased core amplifiers for extended bandwidths at ca. 9 GHz with equal remaining 15-dB midband/dc-gains. Thus both amplifiers use a similar amount of feedback with the results simulated for the proposed dual-loop feedback ticked with  $\diamond$ . Results simulated for the prior-art resistive-only feedback amplifier have been ticked with  $\clubsuit$ , respectively.

Upper sub-picture of Fig. 17 depicts voltage gains for the amplifiers. Small-signal simulation allows extraction of gain as circuit output voltages ( $V_{DB}(\text{out})$ ), as a  $(1-V_p \sim 0 \text{ dB})$  input signal can be used without distortion effects. The plotted data is used to compare peaking near amplifier 3-dB points, where application of the present invention is shown to reduce peaking noticeably for this 15-dB amplifier example. To put this result in perspective two things will be disclosed next: 1) with different element values of the feedback network the improvement



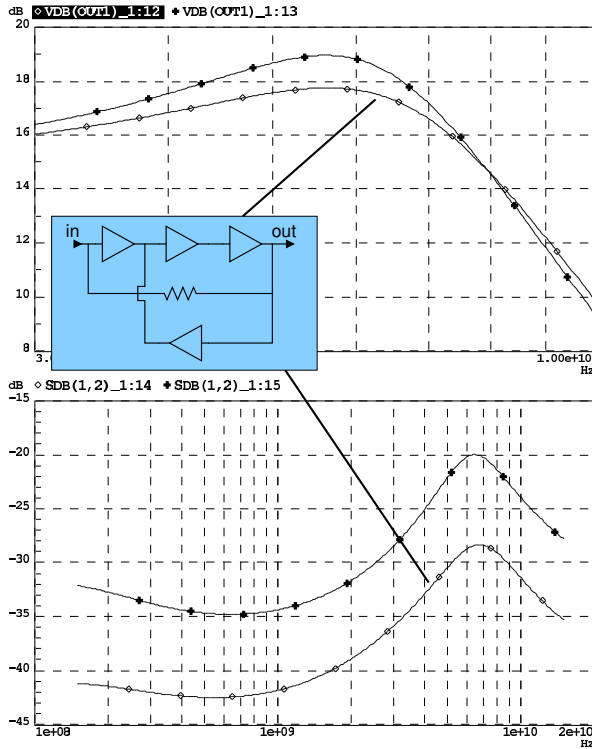


Fig. 17. Simulated comparison of feedback techniques (proposed active feedback= $\diamond$ , prior art resistive-only= $\blacksquare$ ) show a) voltage gain peaking near amplifier 3-dB points, and b) amplifier isolation performances.

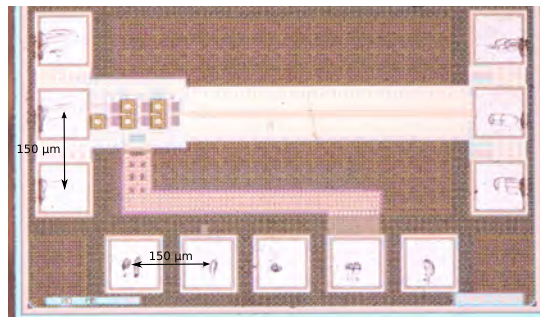


Fig. 18. Microphotograph of the realized UWB LNA shows an active area of  $193\mu\text{m} \times 124\mu\text{m}$ .

obtainable can be increased to ca. 3 dB for this 15-dB amplifier example; and 2) when feedback is increased to produce over 10-GHz bandwidths at 13-dB midband voltage gains, simulation results for the resistor-only feedback amplifier indicate *instability* whereas the proposed circuit maintains stable behavior. Lower sub-picture of Fig. 17 compares simulated two-port isola-

tion parameters  $S_{12}$  for the implemented 15-dB amplifiers with a clear 7-dB improvement indicated for the proposed feedback network technology.

Simulated characteristics for the implemented LNA in Fig. 16 at the nominal biasing point of 14.5 mA from a 1.2-V supply predicts good performance: midband gain is 23.7 dB, bandwidth (BW) reaches 7.2 GHz with good input matching of  $S_{11} = -20.8$  dB at 4 GHz. Simulated noise figures remain below 2.3 dB, and LNA figure-of-merit (FOM) characteristics peaks at 23. The FOM has been used as defined by Borremans et al. (2007):

$$FOM = 20 \log_{10} \left( \frac{Gain(real) BW(GHz)}{Power(mW) (NF(real) - 1)} \right), \quad (3)$$

where Gain stands for insertion gain  $S_{21}$ , BW for amplifier 3-dB bandwidth (in GHz), Power stands for DC power dissipated by the circuit (in milliwatts), and NF is the noise figure given as a real number, i.e., the noise factor of the circuit.

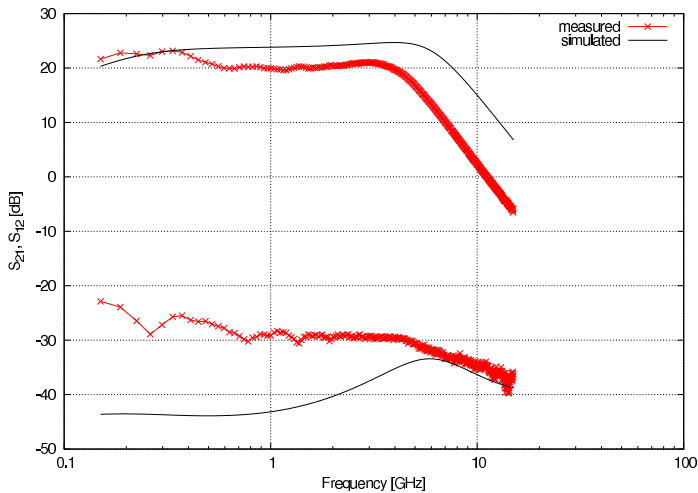


Fig. 19. Comparison of measured and simulated insertion gain ( $S_{21}$ ) and isolation ( $S_{12}$ ) values at the 1.2-V biasing point Tiiliharju & Koivisto (2009) (© 2009 IEEE).

#### 4.3.3 Experimental results

The circuit has been tested in nominal conditions using a supply voltage of 1.2 volts, and a biasing current of 14.5 mA. Testing of the IC shown in Fig. 18 has been done using co-planar wafer probes with a pitch of 150  $\mu\text{m}$ . Measured frequency response performance has been compared to simulated values in Figs. 19-20. Latter of the figures also shows that matching performance is acceptable up to ca. 3 GHz as input return loss values stay below -10 dB. However, the depicted measured values differ from the simulated ones, and this is also seen from tabulated characteristics in Table 3 where noise figures topping 4 dB have been recorded together with  $|S_{11}| = 7$  dB as measured at 4 GHz. The 2-dB NF-value increase from the simulated ones has been verified up to 5 GHz at the three different tabulated operating points, and the measured results have been depicted in Fig. 21. An extra low-noise instrumentation amplifier has been used to drive the spectrum analyzer during the noise measurements as

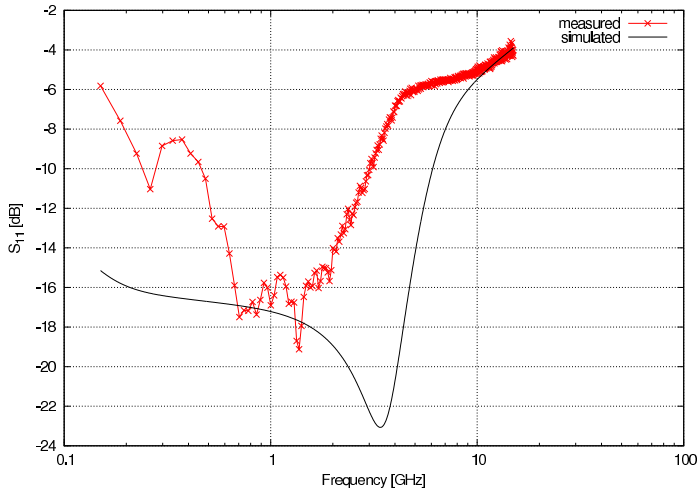


Fig. 20. Comparison of measured and simulated input return loss values at the 1.2-V biasing point Tiiliharju & Koivisto (2009) (© 2009 IEEE).

Tech.	Gain	BW	S11NF			IIP3	freq.	VDD	Power	Area	FOM	Type	Ref.expl.
CMOS	dB	GHz	dB	dB	dBm	GHz	V	mW	mm <sup>2</sup>				
130-nm	20	4.9	-7	4.2	-13	4	1.2	17.4	0.0239	5	feedback	This work	
	19.4	4.5	-7	4.1	-13		1	12.3		6.4			
	17.8	4	-6	5.9	-15		0.8	7.9		2.7			
90-nm	25	0.5-8.2	-7	2	-11	4	2.5	39.0	0.025	15.6	feedback	Zhan & Taylor (2006)	
130-nm	17	1-7	-10	2.7	-4	3	1.4	25.1	0.019	5.9	noise cancel	Ramzan et al. (2007)	
90-nm	15.3	0-6	-10	3.7	NA	4	1	3.4	0.0017	17.7	feedback	Borremans et al. (2007)	
90-nm	24	0.5-6.2	-15	2.7	-5	4	2.7	42.0	0.016	7.9	feedback	Perumana et al. (2007)	
65-nm	15.6	0.2-5.2	-13	3.2	3	4	1.2	21.0	0.01	2.4	noise cancel	Blaakmeer et al. (2007)	
90-nm	12	2-11	-10	5.5	-4	4	1.2	17.0	0.7	-2	noise cancel	Wang & Wang (2006)	

Table 3. Comparison of LNA performances.

this increases reliability of the Y-parameter noise measurements. The measurement setup has also been verified by measuring another amplifier with known noise performance. All other measurements have been done unbuffered, i.e., the proposed LNA has been used to directly drive the equipment.

The plotted NF data together with the recorded gains hints at a layout error at amplifier input, as any noisy resistive parasitics at the LNA output should be masked by its high gain. Nevertheless, the proposed amplifier FOM-performance compares well to state-of-the-art, as it peaks at the 1.0-V biasing point at 6.4. Only one design uses such a low supply voltage, but this has been realized with a more advanced process node. Measured frequency responses at all biasing points shown in Fig. 22 also confirms the claims on stability and good isolation. Only a uniform gain decrease has been recorded with lowering supply voltages, with no discernible degradation in isolation or peaking at passband edge.

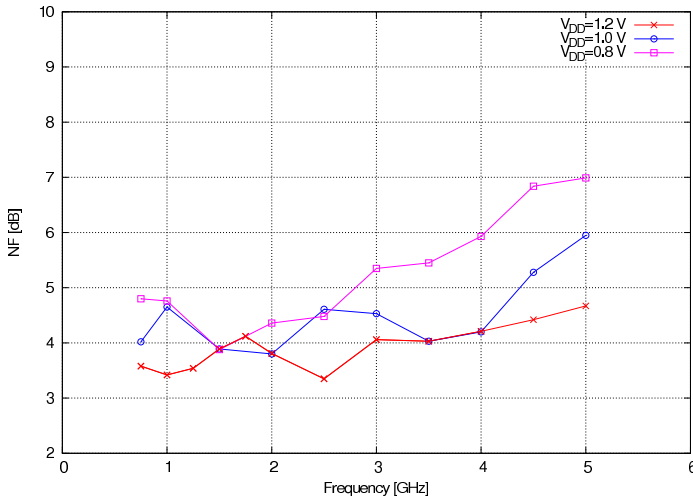


Fig. 21. Comparison of measured NF performance at the 1.2-V, 1.0-V and 0.8-V biasing points.

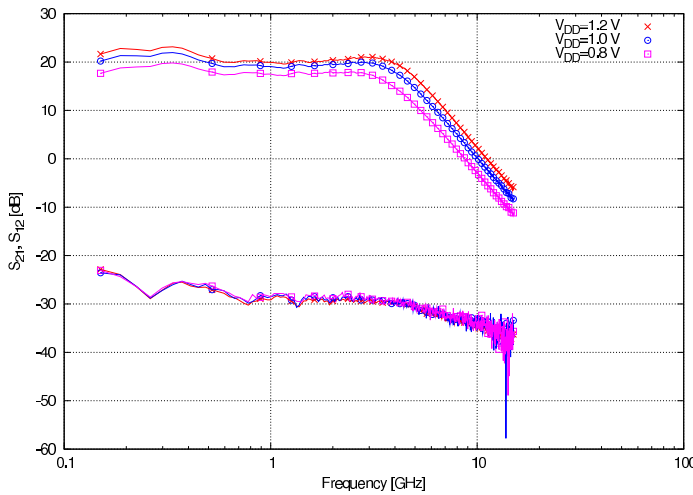


Fig. 22. Comparison of measured insertion gain ( $S_{21}$ ) and isolation ( $S_{12}$ ) performances at the 1.2-V, 1.0-V and 0.8-V biasing points.

### 5. Summary and future work

Successful applications of complementary signal processing to microwave buffers have been studied in this chapter with special emphasis on CMOS. This approach is justified by CMOS scaling to the nanometer domain, which makes it possible to use this very economical technology in the microwave domain. However, first section has elaborated on a complementary bipolar process and its possible application for basestation buffering purposes, an application which is perhaps better served with this high-voltage process. Second section has discussed

integrated baluns, which naturally has taken this text to the third section on LNAs where different topologies compatible with modern nanoscale CMOS technologies have been studied. To summarize, it seems that there is a substantial benefit in using complementary analog signal processing techniques, however, parasitics compensation is a demanding design task in the higher operating bands.

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